FINAL PROJECT REPORT

ON

"LOCALLY CONNECTED ADAPTIVE GABOR FILTER FOR REAL TIME MOTION COMPENSATION"

ONR GRANT NUMBER: N00014-94-1-0007

This report is submitted to the Office of Naval Research On June 25th, 1997

Principal Investigator: Hua Harry Li, Ph.D.
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Summary

The purpose of this study is to investigate and to develop locally connected dynamic Gabor filter for real time illumination-invariant motion compensation. This work can be employed in various applications, including potential applications in image stabilization.

In particular, this research project consists of the phase of theoretical study, algorithm development, and VLSI (Very Large Scale Implementation) chip design. The chip design process begins with the system level design which first translates the mathematical formulation to hardware requirement and specifications, then the subsystem level, and basic building block designs are performed together with circuits simulations prior to the physical VLSI circuits layout. Then the designed chip, Gabor filter, is submitted to MOSIS for fabrication on double poly 2.0 micro CMOS technology.

In order to verify the mathematical formulation, software simulation in C programming language is first performed. The source code is documented and submitted to ONR as one of the progress reports, in addition an user manual is also submitted to ONR for reference purpose.

The VLSI Gabor chip is fabricated, then the post-fabrication testing and verification are conducted. The electronics characteristics are measured against the designed specification, silicon modifications are made, bugs are removed. A functional, working chips are obtained.

During the process of this undertaking, one edited book, "Vision Chips: Implementing Vision Algorithms with Analog VLSI Circuits," (Co-edited by Christof Koch of California Institute of Technology) is published by IEEE CS Press, part of the findings is reported in IEEE Journal of Solid-State Circuits, February 1997 issue. And some related theoretical results are also published in IEEE Conference on Circuits and Systems 1996. Towards the end of the project, the working VLSI chips and a prototype board performing analog convolution are demonstrated in IEEE Conference on Neural Networks in Washington D.C. in 1996.

The current fabricated VLSI chip is only a small part of the original proposed Gabor filter due to the limited available silicon and the budget constraint. However the concept demonstrated here is well taken and accepted. In May 1996, IEEE Spectrum published cover-story, "Toward An Artificial Eye," our work was cited in the section of "To Probe Further" on page 68.

Through this research project, both Master level graduate students and Ph.D. level graduate students are participated and three Master Thesis are produced as listed in details in this report. This research project not only helps the advancement of the understanding of the engineering practice and scientific research, but also provides an opportunity to allow better graduate education.

I. The Objective of This Study

The objectives of this study as described in the proposal is to investigate and to develop locally connected dynamic Gabor filter for real time illumination-invariant motion compensation. This work can be employed in various applications, including applications in image stabilization. The VLSI silicon implementation of the algorithm is the focus of this research. The mathematical formulation and circuits design are translated to the physical VLSI chip realization on double poly 2-micro CMOS technology.

II. The Accomplishment

The accomplishment of this project include

(1) the development and verification of the illumination-invariant algorithm;

(2) prototyping of software testing programs, verification functions and user manual;

(3) design and implementation of hardware proof-of-concept analog convolution board; and

(4) VLSI system level, subsystem level, and basic building block design;

(5) physical layout, prelayout and post layout SPICE simulation;

(6) analog VLSI chip fabrication through MOSIS, and final validation of the design;

(7) Publication of the findings in Journal of IEEE Solid State Circuits, and edited book "Vision Chips, Implementing Vision Algorithms with Analog VLSI Circuits," published by IEEE CS Press, and graduate study thesis. The itemized summary of these findings and accomplishment is given in the following sections.

2.1 Development of Algorithms

One of the unique features of this study is the mathematical formulation of Gabor Transform that allow illumination-invariant optical flow computation, please see the previous progress reports and the proposal for the details of the mathematical equations. In addition, the algorithm is developed in such a way of allowing relatively easy implementation in analog VLSI hardware. The related technical documentation, "Selection of Gabor Kernels for Image Processing," a graduate Master Thesis by Xiaohui Meng, was also produced as a part of this effort and the effort of software simulation and verification.

2.2 Testing and Evaluation Software

Software C-programming is first employed to test the algorithm before engaging VLSI design and implementation. These programs demonstrate the computation of optical flow, orientation selectivity, spatial-frequency selectivity, and the utilization of both orientation selectivity and spatial frequency selectivity for optical flow computation.

Based on the frequency selectivity, motion information from both very low frequency which is usually connected to ego motion and band-passed frequency which is usually connected to the object motion can be derived, especially for motion compensation purpose. This allows the possibility of removing motion due to the ego motion, or camera motion.

2.3 Proof-of-Concept Hardware Prototype Board

After the mathematical formulation and evaluation of the algorithm, and the verification of the software development phase, we have designed and built a proof-of-concept hardware prototype board using the standard off-the-shelf components. The purpose of this board is to further confirm the idea of analog computing of Gabor Transform and to provide a test bed as a reference for the next phase of the project, VLSI chip design. The designed and prototyped board is ISA based board, which does analog convolution with kernel size of 3-by-3, 5-by-5 and 7-by-7. The kernel weights can be modified for either LoG (Laplacian of Gaussian) or Gabor function. Given in Appendix A is the photo of the prototype board.

The technical details of the design was given in a documentation, "Analog Two Dimensional Convolution for Image Processing," a graduate student Master Thesis by Donald Symes. A fully functional, ISA bused based, analog convolution board was exhibited at 1996 IEEE Conference on Neural Networks, Washington D.C.

2.4 The Prototyping, Simplified Version, Working VLSI Chip

The VLSI chip is designed and fabricated using double poly 2.0 micro CMOS technology. The chip is fabricated by MOSIS service. Post fabrication testing, and verification are conducted, design iteration and modification is performed. Silicon bugs are removed and design enhancement is achieved. The fully functional, working chip of reduced functionality is realized (video buffer part), see Appendix B for the photo of one fabricated chips during the process of this effort.

The fabricated VLSI chip does two dimensional Gabor convolution which is the key operation of the proposed system. To realize the entire system in silicon, considerable resources have to be added to allow the physical realization of all the functionality. With this small simplified version, the purpose of proof-of-concept has already been achieved, the rest of the implementation can follow the same design procedure. Part of this silicon realization is reported in our previous Progress Report, and also in a documentation, "Analog VLSI Implementation of a Gabor Convolution for Real Time Image Processing," a master thesis by Laszlo Moldovan.

Although the current fabricated VLSI chip is only a small part of the original proposed Gabor filter due to the limited availability in silicon and the budget constraint, the concept demonstrated here is well taken and accepted. In May 1996, IEEE Spectrum published cover-story, "Toward An Artificial Eye," our related work as part of this research effort was cited in the section of "To Probe Further" on page 68. See Appendix H.

2.5 Produced Graduate Study Thesis

During the process of this project, both Master level graduate students and Ph.D. graduate student are involved. Three Master Thesis are produced,

1. "Selection of Gabor Kernels for Image Processing," by Xiaohui Meng, see Appendix C.
2. "Analog Two-Dimensional Convolution for Image Processing," by Donald Symes, see Appendix D.
3. "Analog VLSI Implementation of a Gabor Convolution for Real Time Image Processing," by Laszlo Moldovan, see Appendix E.

III. The Technical Publications

The technical publications as a part of the research effort includes both one edited book on VLSI chips for vision computing, and IEEE journal paper, IEEE Conference papers, and graduate student thesis described as follows.

3.1 A IEEE CS Press Book

An edited book, "Vision Chips: Implementing Vision Algorithms with Analog VLSI Circuits," with Christof Koch of California Institute of Technology, IEEE CS Press, ISBN 0-8186-6491-6, 1995. Please see Appendix F

3.2 Publication at IEEE Journal of Solid State Circuits

A published work, "A Rail-to-Rail, Constant Gain, Buffered Op-Amp for Real Time Video Applications," IEEE Journal of Solid-State Circuits, pp. 169-176, Vol. 32, No. 2, Feb. 1997. See Appendix G.

3.3 Publication at IEEE International Conference

A published work, "A Rail-to-Rail Constant Gain Buffered Op-Amp for Real Time Video Applications," by Laszlo Moldovan and Hua Harry Li, IEEE Conference on Circuits and Systems, Atlanta, 1996.

3.4 Technical Exhibition at IEEE International Conference

The exhibition of the prototype board and the VLSI chips was made at IEEE Conference on Neural Networks in Washington D.C. in 1996.

IV. The Future Directions

The current silicon realization is only a small fraction of the entire system, there is a need to actually build the whole system, and provide a testing bed as a PCI based board environment to allow the chip fully operations under GUI (Graphics User Interface). This will close the gap of the theory and the real product. Because of the size and the complexity of the chip, we are only able to test the Video Buffer part of the realization, in order to test entire chip, the Realtime Gabor convolution, it is needed to have a PCI based board built for this purpose.

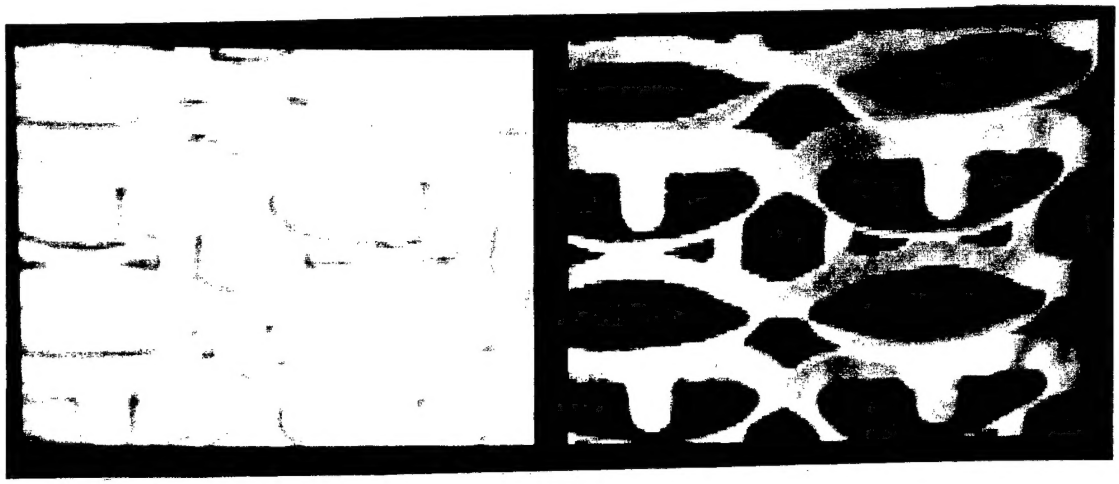
It appears to us that the concept of orientation selectivity and spatial frequency selectivity can be utilized for better video compression applications with multi-resolution variable bit rate video.

The end.

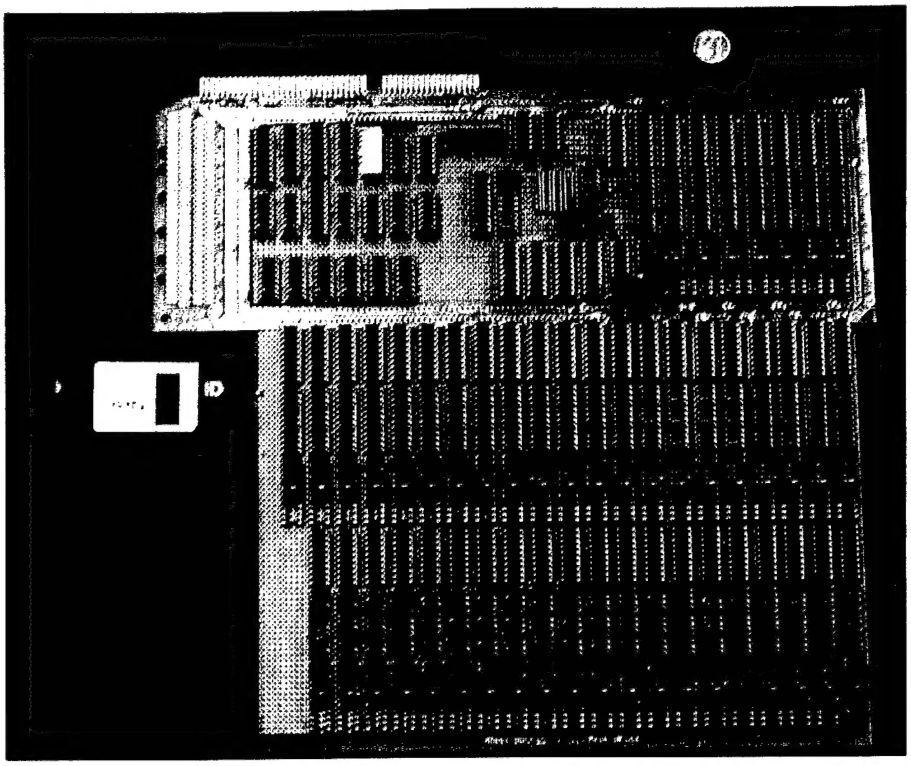
APPENDIX A

A Prototype Board As a Proof-of-Concept Board for analog 2D Convolution

PROOF OF CONCEPT BOARD: ANALOG CONVOLUTION STANDARD OFF-THE-SHELF COMPONENTS

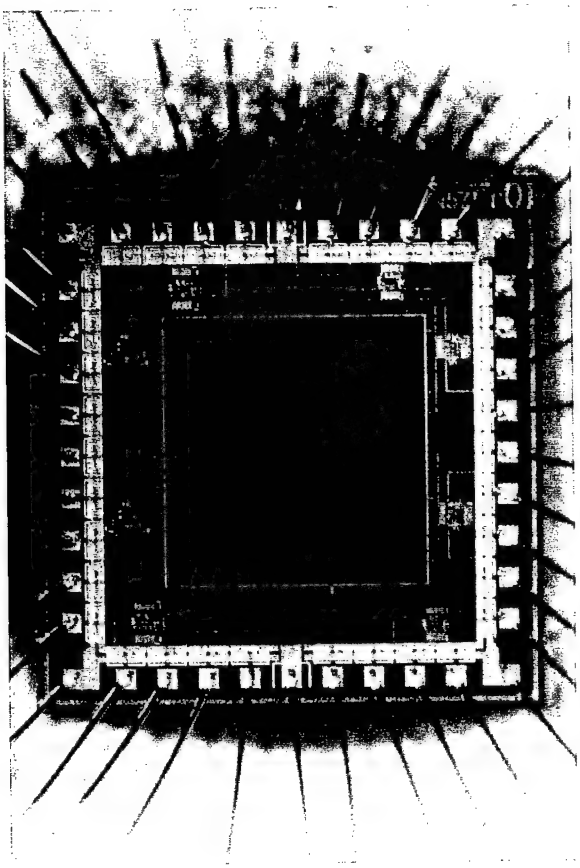


Convolution with a 7x7 kernel Original Image



APPENDIX B

One of the Fabricated Chips



APPENDIX C

A Cover Page of Master Thesis
"Selection of Gabor Kernels for Image Processing," by Xiaohui Meng

SELECTION OF GABOR KERNELS FOR IMAGE PROCESSING

by

XIAOHUI MENG, B.S.Engr.

A THESIS

IN

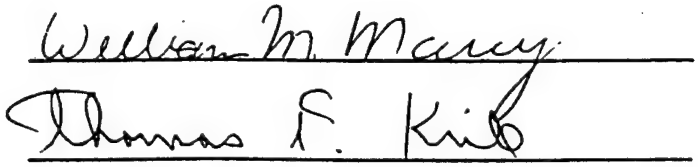
COMPUTER SCIENCE

Submitted to the Graduate Faculty
of Texas Tech University in
Partial Fulfillment of
the Requirements for
the Degree of

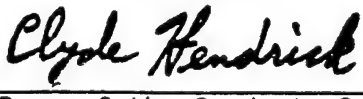
MASTER OF SCIENCE

Approved

Chairperson of the Committee



Accepted



Dean of the Graduate School

December, 1994

APPENDIX D

A Cover Page of Master Thesis
"Analog Two-Dimensional Convolution for Image Processing," by Donald Symes

Analog Two-Dimensional Convolution for Image Processing

Master's Thesis

Donald A. Symes

Committee
Dr. Hua Li - Chair
Dr. Donald C. Wunsch II
Dr. W. J. B. Oldham

November 1994

Computer Science Department
College of Engineering
Texas Tech University

APPENDIX E

A Cover Page of Master Thesis
"Analog VLSI Implementation of a Gabor Convolution for Real Time Image Processing," by Laszlo Moldovan

ANALOG VLSI IMPLEMENTATION OF A GABOR CONVOLUTION FOR REAL TIME IMAGE PROCESSING

by

LASZLO MOLDOVAN, B.S., M.S.E.E.

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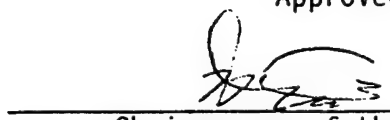
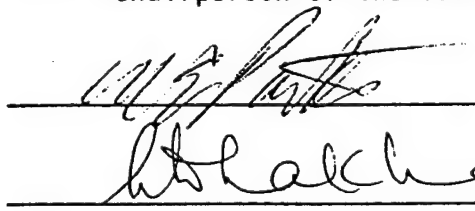


Chairperson of the Committee



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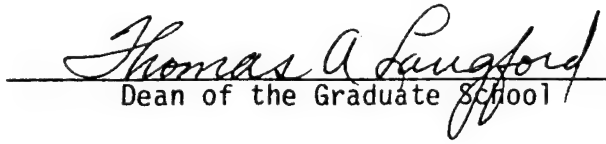


Dean of the Graduate School

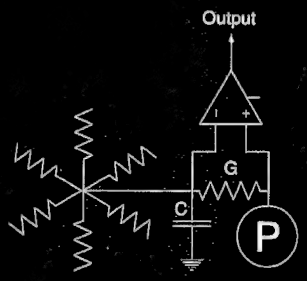
May, 1996

APPENDIX F

An edited book, "Vision Chips: Implementing Vision Algorithms with Analog VLSI Circuits," with Christof Koch of California Institute of Technology, IEEE CS Press, ISBN 0-8186-6491-6, 1995

VISION CHIPS
Implementing Vision Algorithms with Analog VLSI Circuits

Christof Koch and Hua Li



IEEE Computer Society Press

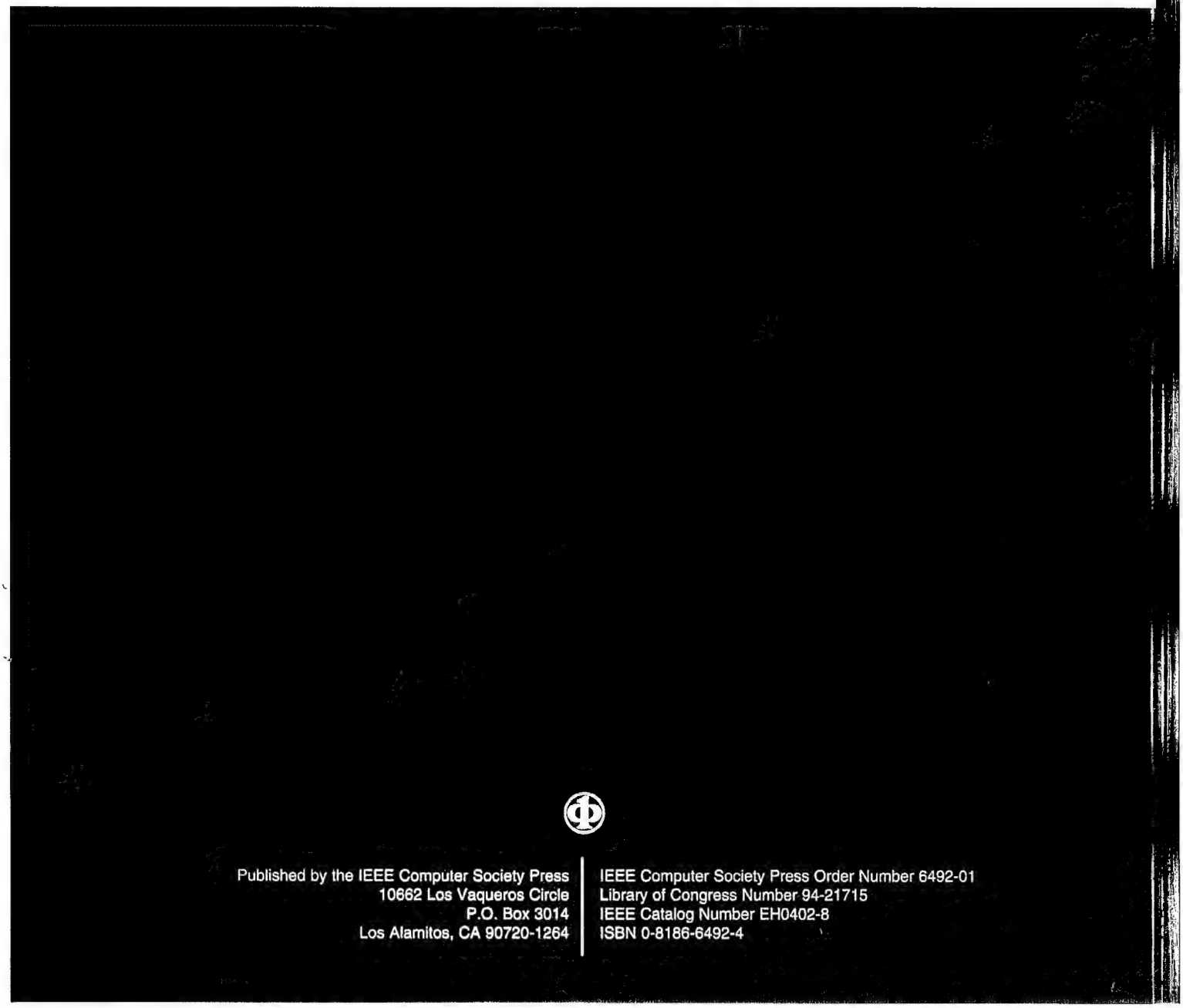
The Institute of Electrical and Electronics Engineers, Inc.

VISION CHIPS:
Implementing Vision Algorithms with Analog VLSI Circuits

edited by Christof Koch and Hua Li

Recent research has resulted in an improved understanding of the operations underlying visual processing, which has allowed researchers to create a large number of well-studied algorithms. However, conventional computer implementations of these algorithms are usually very slow, even on large machines. At the same time, researchers—using CMOS VLSI technology—have designed special-purpose analog circuits, based directly or indirectly on neurobiological circuits, that implement a number of early vision algorithms in real time. In such smart-sensor paradigms, image acquisition is combined with image processing onto a single chip.

This book examines recent advances in implementing early vision algorithms onto special-purpose CMOS analog vision chips as well as charge-coupled devices (CCDs). The text begins with a review of the fundamental problems of early vision. It goes on to describe particular circuits that implement spatio-temporal filtering to remove noise, emphasize features (such as edges) in the image, estimate optical flow, compute depth, and carry out figure-ground segregation.



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APPENDIX G

A published work, "A Rail-to-Rail, Constant Gain, Buffered Op-Amp for Real Time Video Applications," IEEE Journal of Solid-State Circuits, pp. 169-176, Vol. 32, No. 2, Feb. 1997

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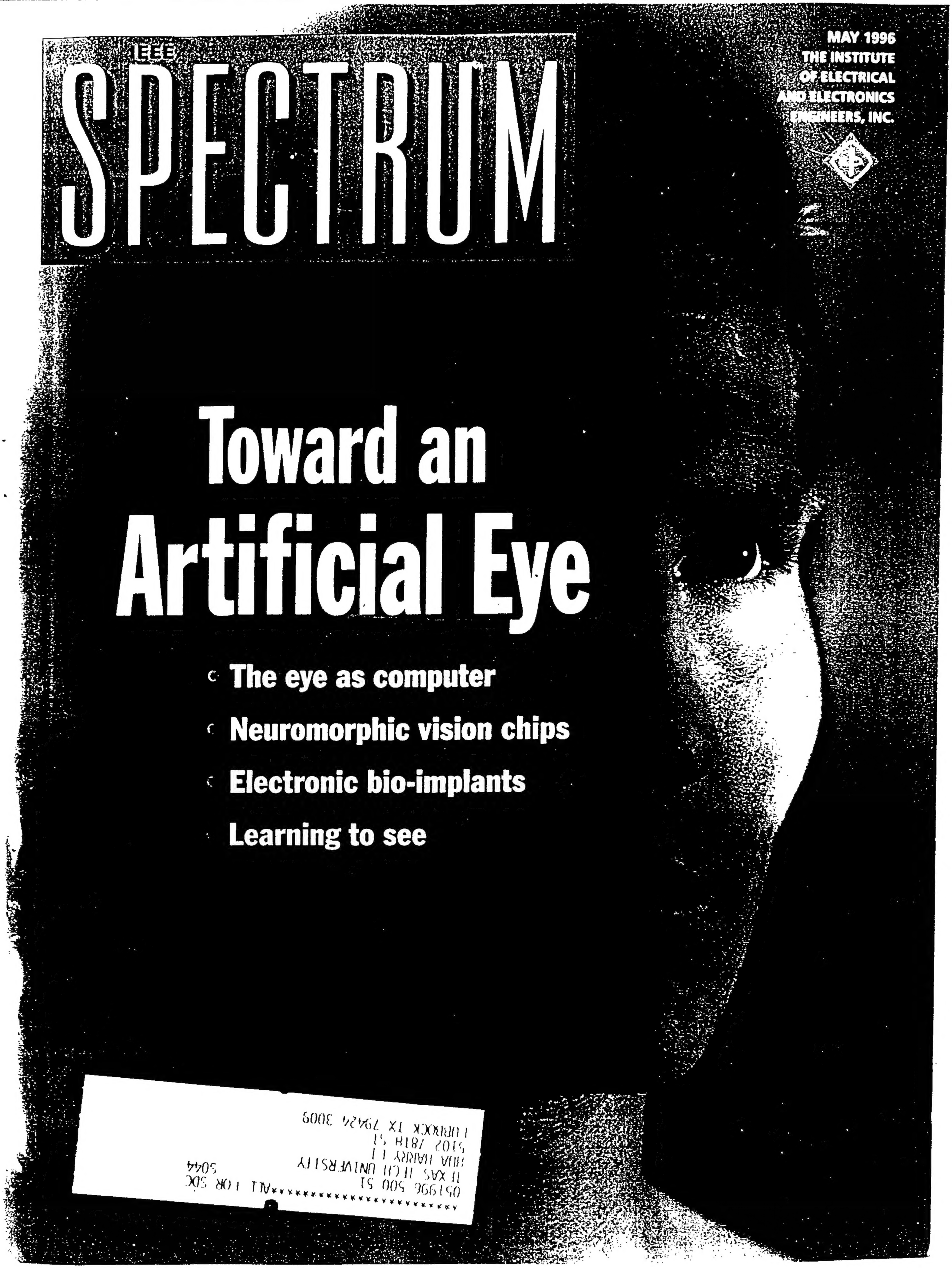
APPENDIX H

In May 1996, IEEE Spectrum published cover-story, "Toward An Artificial Eye," our related work as part of this research effort was cited in the section of "To Probe Further" on page 68.

IEEE
SPECTRUM
MAY 1996
THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.



Toward an Artificial Eye

- The eye as computer
- Neuromorphic vision chips
- Electronic bio-implants
- Learning to see

vision chips," pp. 38–46]. The two systems achieved 100 and 93 percent accuracy, respectively.

3, 4: at ease, password approved

A pose-invariant face recognizer was developed by one of us (Beymer), so that the person to be recognized might face the camera in a less constrained and more natural way. The system uses 15 views per object, to covers many more out-of-plane rotations. If the object is a face, its owner can look around and still be analyzed visually.

As in the two template-matching networks, translation, scale, and image-plane rotation are factored out by first detecting features of the eyes (and nose) and then using these features to register the input with the model views. Using a small database of 620 images (62 people, 10 test views per person), the recognition rate was 98 percent. The test images were at a variety of image rotations, both in and out of the image plane.

The fourth system tries to verify that a person looks like whoever she claims to be, rather than match up her image to one in a database. For the first task, we humans recall a notion of what that person looks like and compare it with the presented image. For the second, we mentally scan a gallery of faces we know.

The system, developed at MIT by Raquel Romano and one of us (Beymer), runs in real time on a low-end Indy computer from Silicon Graphics Inc., Mountain View, Calif., using the IndyCam CCD camera to capture the image.

This recognition system will be tried out in its birthplace: it will stand guard at MIT's Artificial Intelligence Laboratory. Each user types in a log-in name and then, rather than typing in a password, is prompted to look at a camera, for vetting by the system.

Even harder than recognizing an isolated specific object is detecting an object within a cluttered image. For instance, it can be very hard to notice whether a crowd contains a given face. For computers, this task is even more difficult. Nonetheless, a system developed in 1993 by Kah-Kay Sung and one of us (Poggio) at MIT has been successfully trained to find faces, eyes, and other objects by incorporating a vastly larger and differing type of image database.

The system's ability in action to locate frontal images of faces is conveyed by Fig. 5. Part of the system's strength is that a multitude of examples—54 000 in all—was used for training. Interestingly, though, only 1000 of them were real in the sense of being taken from snapshots of actual people; 3000 of the test images were part of virtual examples, of which more shortly.

The vast majority of the images were negative example images: an immense grab bag of 50 000 patterns, each defined to the computer as "non-face." These were mostly cut-off views of torsos, hands, and other parts of individuals and groups, as well as some random shots of the world. This is a twist to the supervised learning scenario discussed so far: including "incorrect" examples (but identifying them as such) added a different, and in some ways more effective, pedagogic technique to the basic idea of a teacher showing a student a correct I/O example. Moreover, a second type of "incorrect" example set was included: images that the system had mistakenly identified as faces.

To probe further

Toward an artificial eye, pp. 20–29

For a superb overview of the overlap between computational and biological approaches to the study of the nervous system, particularly vision, read *The Computational Brain* by Patricia S. Churchland and Terrence J. Sejnowski (MIT Press, Cambridge, Mass., 1992). A similarly rich volume of collected essays, many tutorial, is *Neuro-Vision Systems: Principles and Applications*, edited by Madan M. Gupta and George K. Knopf (IEEE Press, Piscataway, N.J., 1994).

The Low Vision Enhancement System is detailed in author Massof and co-workers' "Low-Vision Enhancement System," Johns Hopkins APL Technical Digest, Vol. 15, no. 2, 1994, pp. 1–6.

Details on the European Community–funded Portable Optoelectronic Vision Enhancement System can be found in "POVES: A Portable Optoelectronic Vision Enhancement System," a paper by W. Zagler and co-workers in the Proceedings of the 2nd TIDE Congress, Paris, IOS Press, 1995, pp. 352–55.

Electronic resources, links, and texts of the American Federation for the Blind can be found at gopher://gopher.afb.org:5005/. The Royal National Institute for the Blind has an excellent home page, with numerous links and documents, at www.rnib.org.uk/. The Vision Science Home Page with links to numerous vision reseach organizations is http://vision.arc.nasa.gov/VisionScience/VisionScience.html.

The computational eye, pp. 30–37

A physiological view of retinal function is presented in *The Retina, an approachable part of the brain*, by John E. Dowling (Belknap Press of Harvard University Press, Cambridge, Mass., 1987). For more on cellular nonlinear networks (CNNs) in general, look up three papers in *IEEE Transactions on Circuits and Systems*: L. O Chua and L. Yang on "Cellular neural networks," (CAS-35, pp. 1257–90,1988); L. O. Chua and T. Roska, "The CNN paradigm," (CAS 40, pp. 147–56, 1993); and T. Roska and L. O. Chua, "The CNN Universal Machine: An analogic array computer" (March 1993). Details on how to generate neuromorphic models in the CNN may be found in an upcoming (1996) paper by A. Jacobs, T. Roska, and Frank Werblin, titled "Methods for constructing physiologically motivated neuromorphic models in CNNs" (*International Journal of Circuit Theory and Applications*, Vol. 24, May issue). In the 1995 volume of the same journal, Werblin, Roska, and Chua write on "The analogic cellular neural network as a bionic eye" (Vol. 23, pp. 541–69).

Neuromorphic vision chips, pp. 38–46

The bible of the neuromorphic circuit engineer is Carver Mead's *Analog VLSI and Neural Systems* (Addison-Wesley, Reading, Mass., 1989). In addition, more than 40 important papers have been collected by editors Cristof Koch and H. Li in *Vision Chips: Implementing Vision Algorithms with Analog VLSI Circuits* (IEEE Computer Society Press, 1994). Almost all of the chips discussed here were initially designed and fabricated through the U.S. government–supported silicon clearing house, Mosis (http://www.isi.edu80/mosis/). A fairly comprehensive Web site with an up-to-date description of analog and digital vision chips and with links to the home pages of many academic groups working in this area can be found at http://www.eleceng.adelaide.edu.au/Groups/GAAS/Bugeye/visionchips. Finally, the National Science Foundation sponsors an annual three-week-long, hands-on summer course on neuromorphic engineering in Telluride, Colo. For information, see http://www.klab.caltech.edu/~timmer/telluride.

Ocular implants for the blind, pp. 47–53

For an account of recent experiments studying the responses of blind human volunteers to electrical stimulation of the retina, see "Visual Perception Elicited by Electrical Stimulation of Retina in Blind Humans" by Mark Humayun and co-workers in *Archives of Ophthalmology*, Vol. 114, pp. 40–46, 1996. The earlier work at the California Institute of Technology on nonbiological microchips that mimic some aspects of retinal function is recounted in "The Silicon Retina" by Misha Mahowald and Carver Mead in the May 1991 *Scientific American*, pp.76–82. A detailed experimental study of retinal response to electrical stimulation, intended to guide the design of an ocular implant, is reported in "Single Unit Recording Following Extracellular Electrical Stimulation of Rabbit Retinal Ganglion Cell Bodies," by